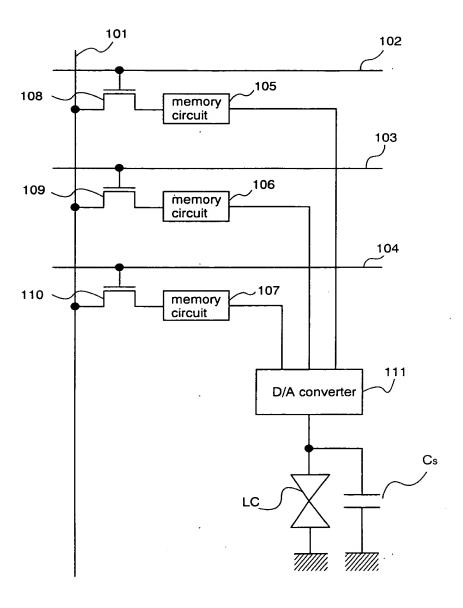
Fig. 1



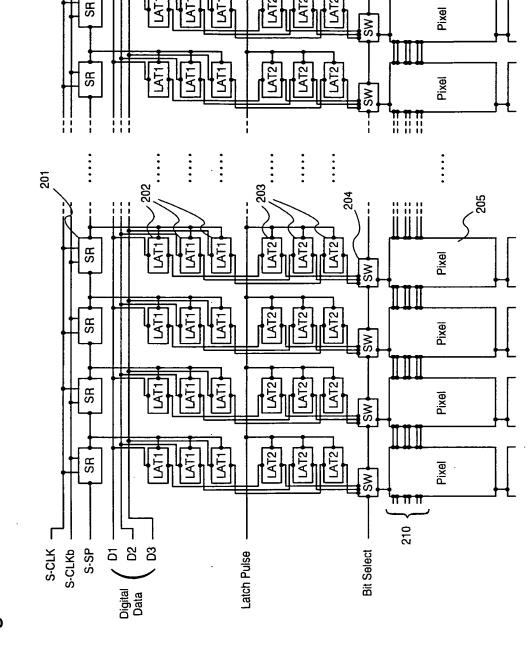


Fig. 2

Fig. 3A

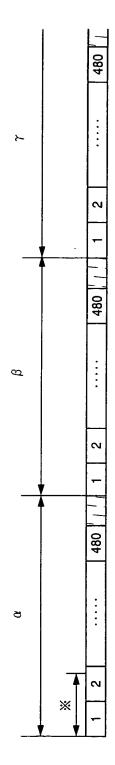


Fig. 3B latch data transferring period

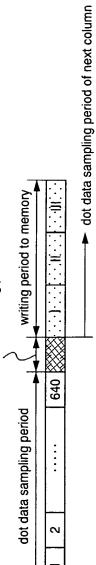
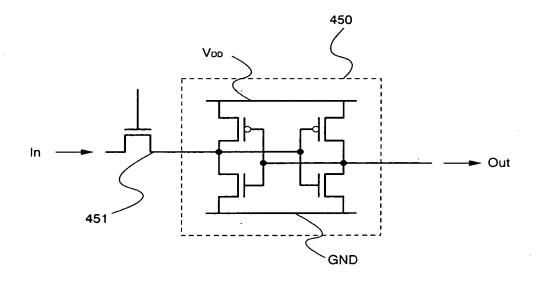


Fig. 4



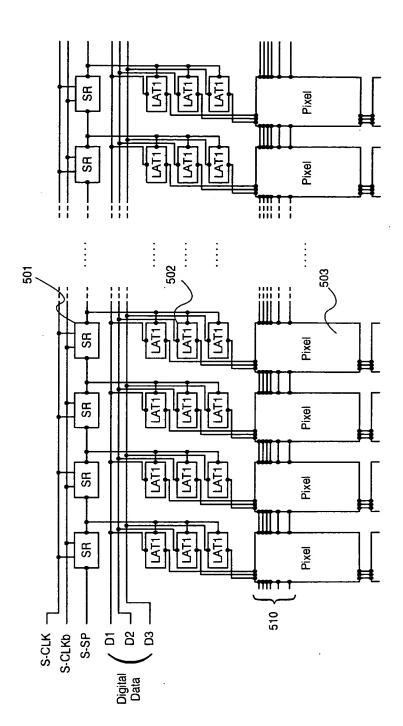


Fig. 5

Fig. 6

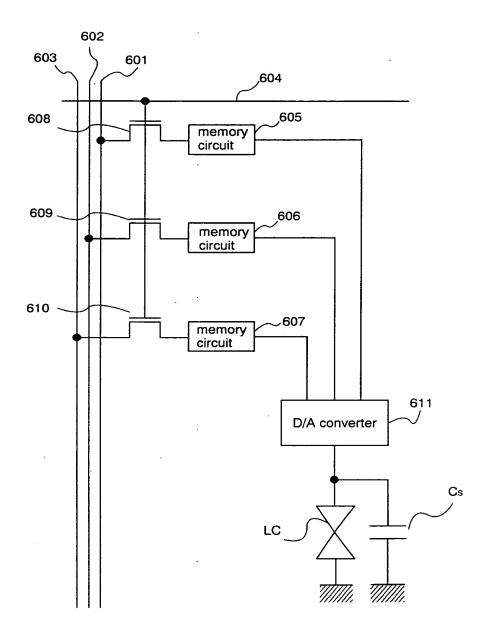
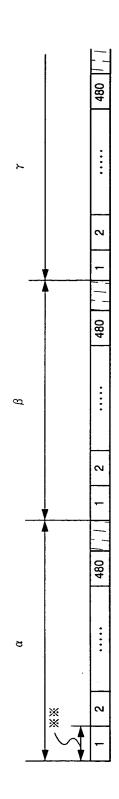


Fig. 7A



-ia. 7B

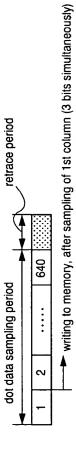


Fig. 8

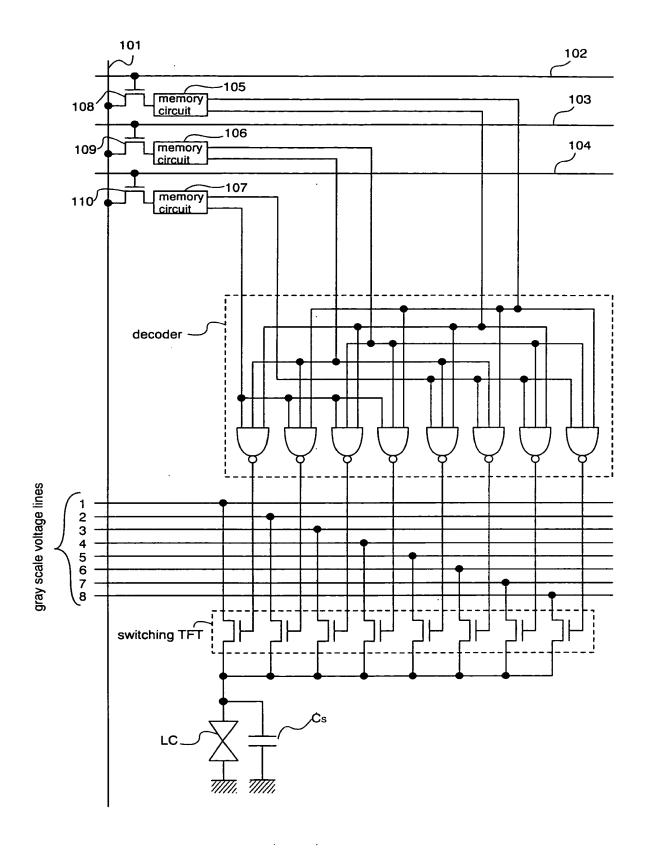
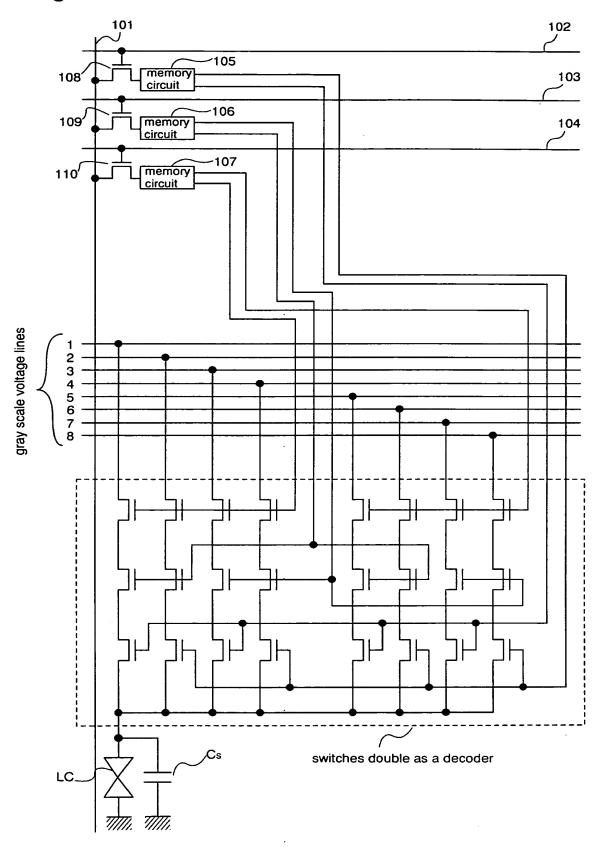
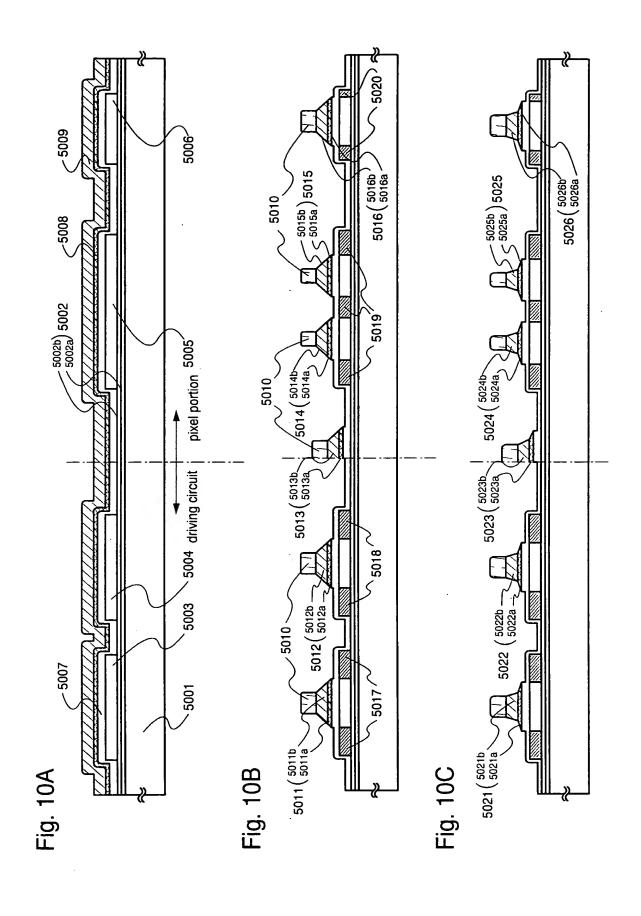
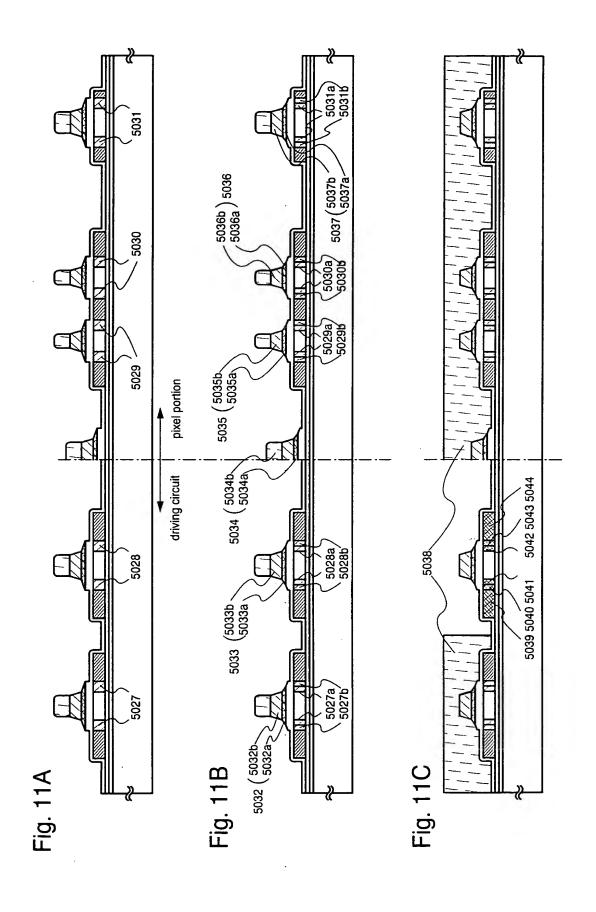
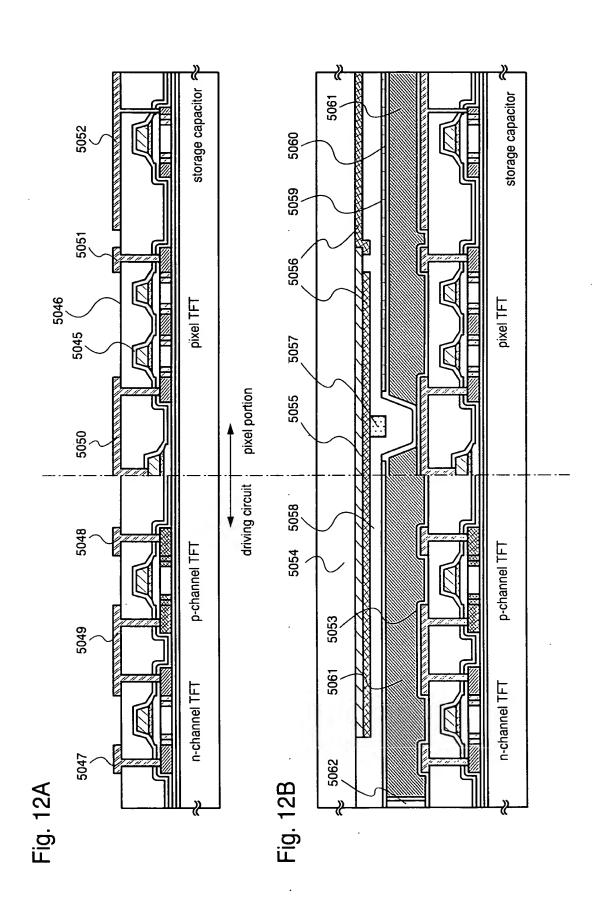


Fig. 9











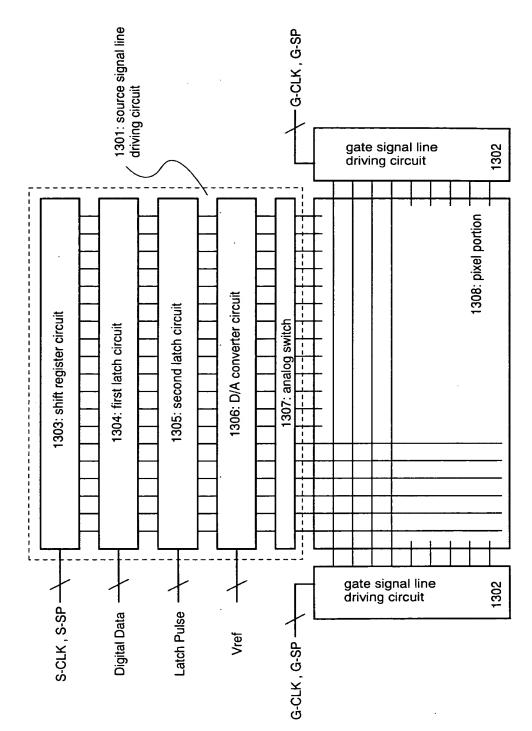
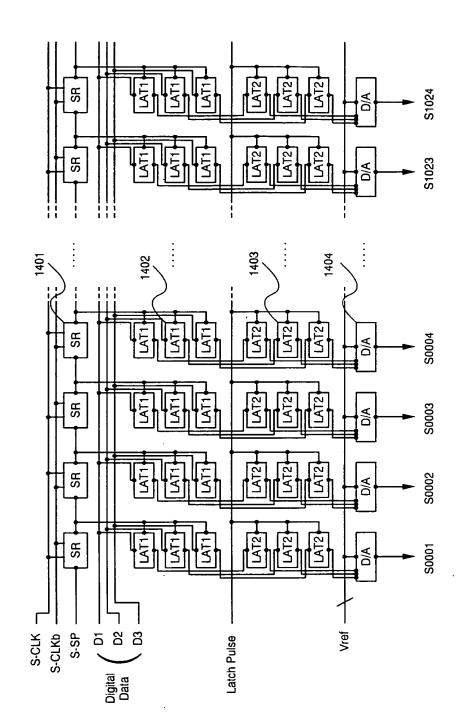
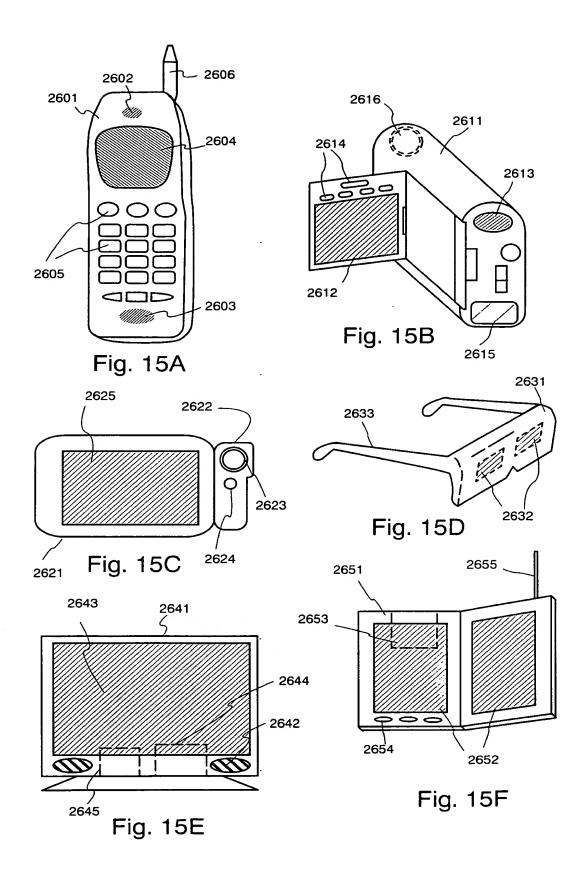


Fig. 14





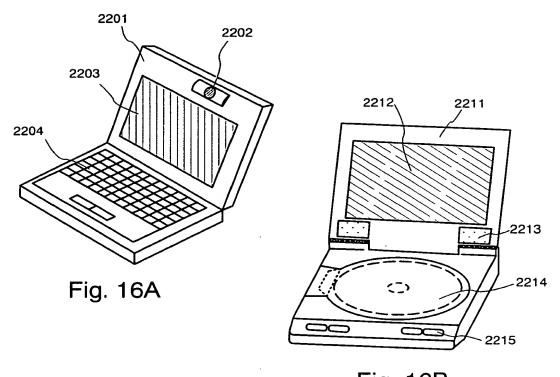


Fig. 16B

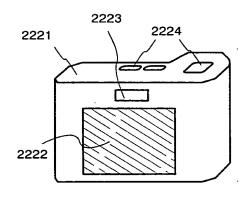


Fig. 16C

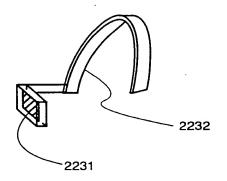


Fig. 16D

Fig. 17

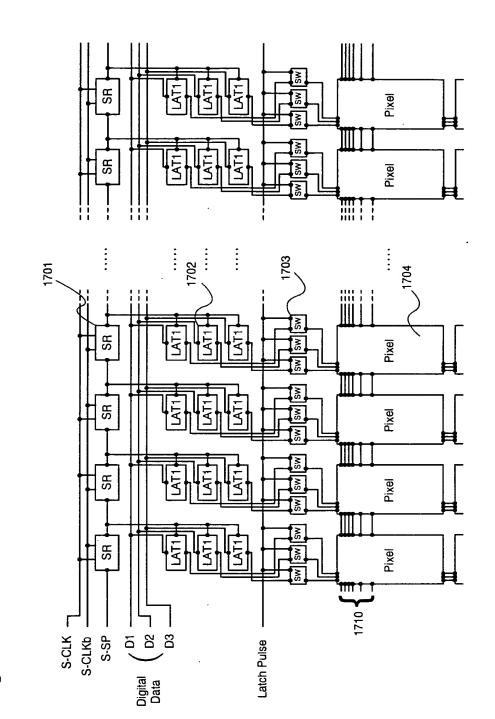


Fig. 18A

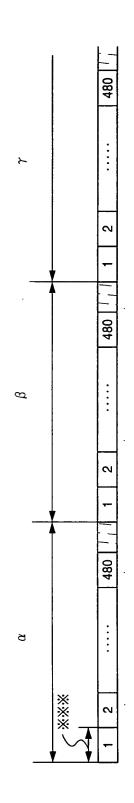
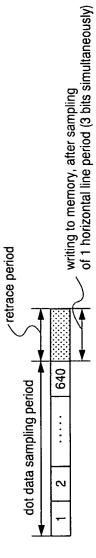


Fig. 18B



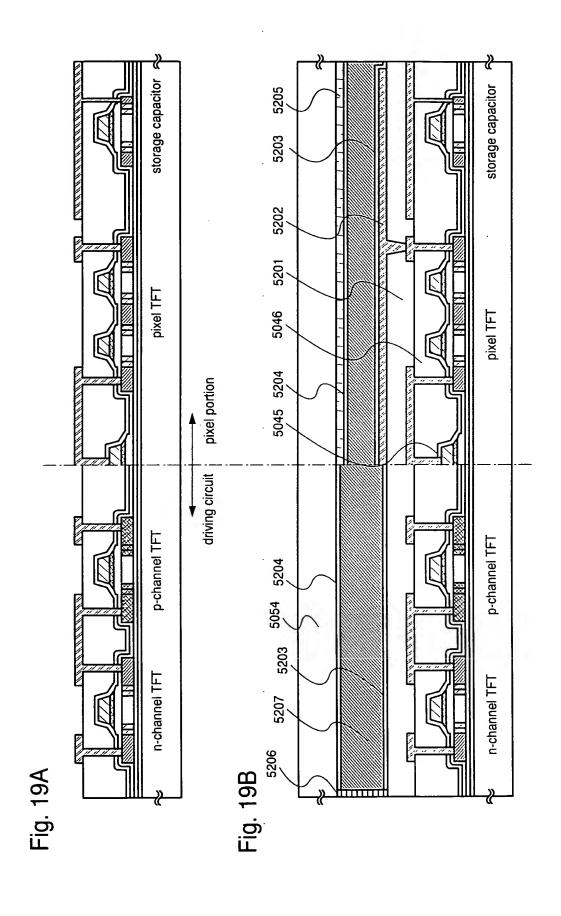


Fig. 20

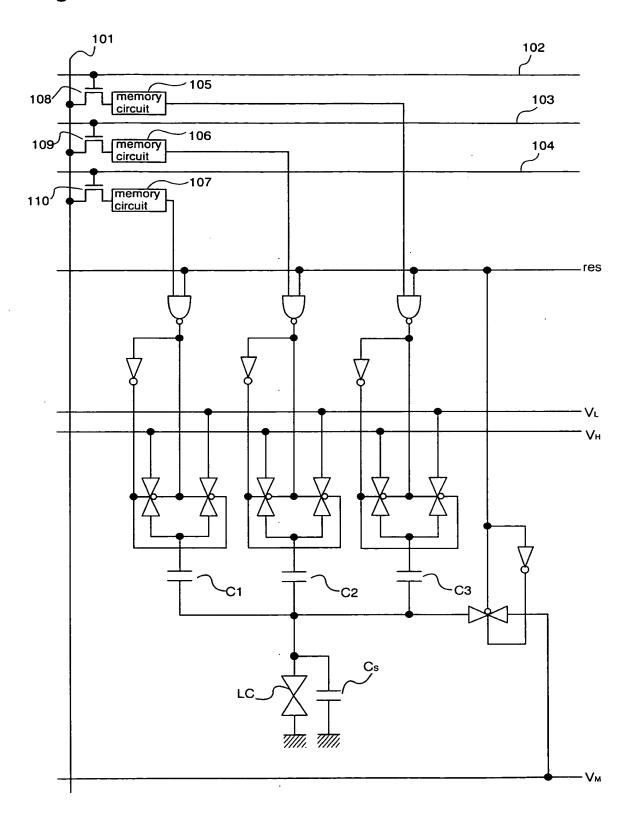
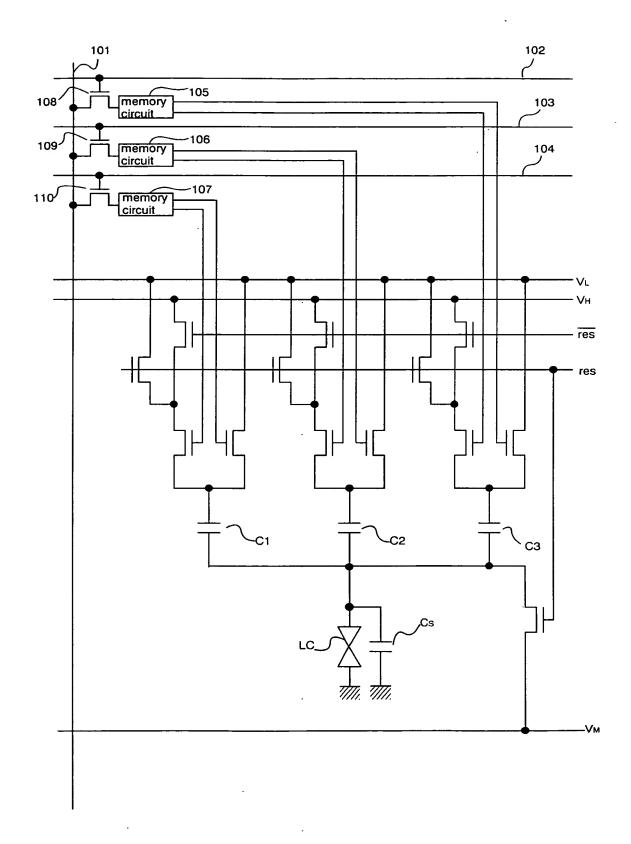


Fig. 21



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Fig. 22

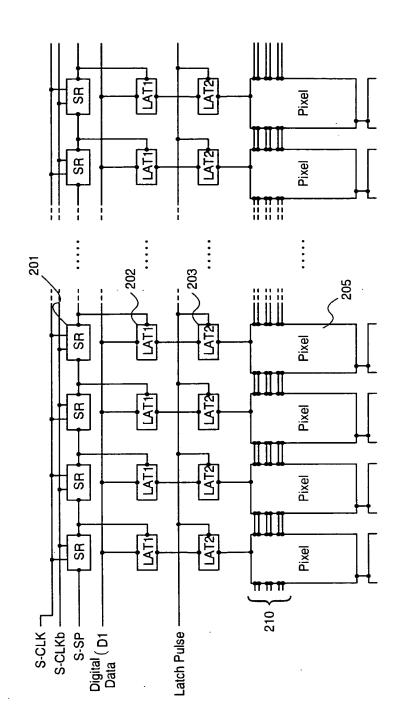
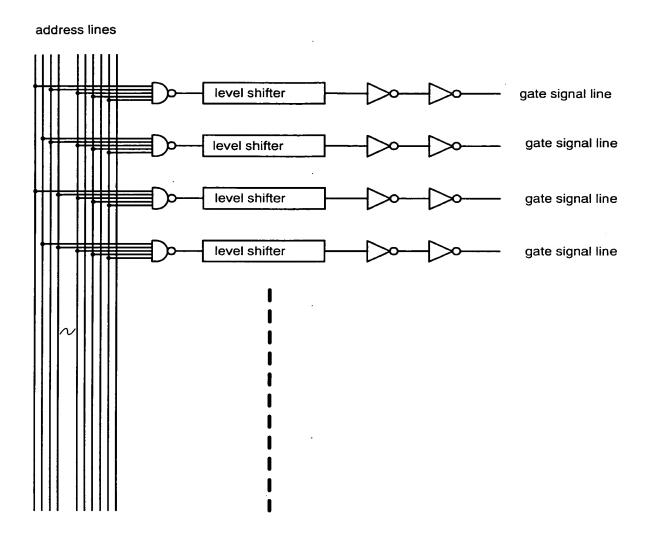
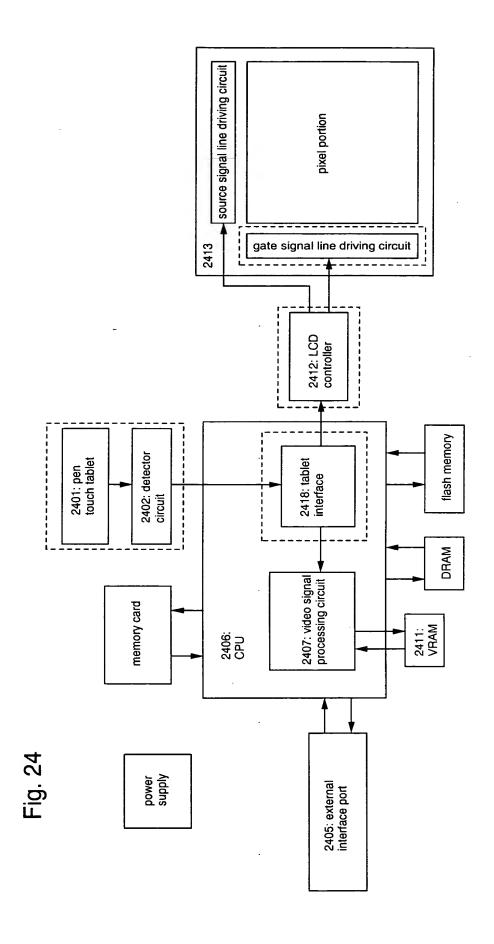
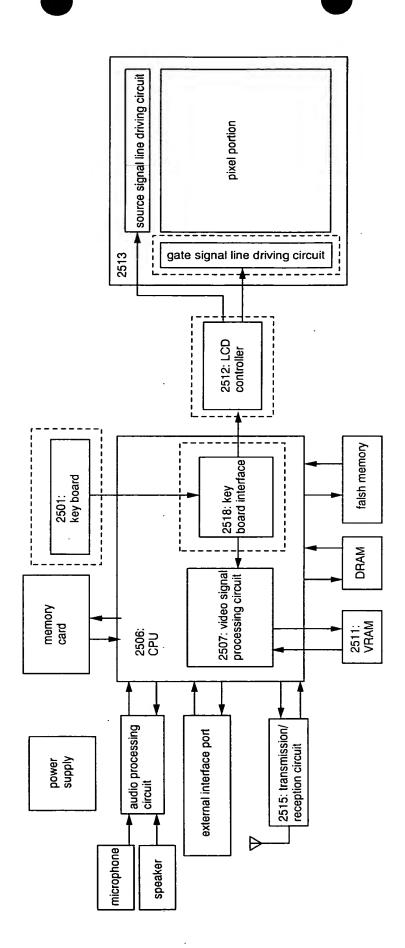


Fig. 23

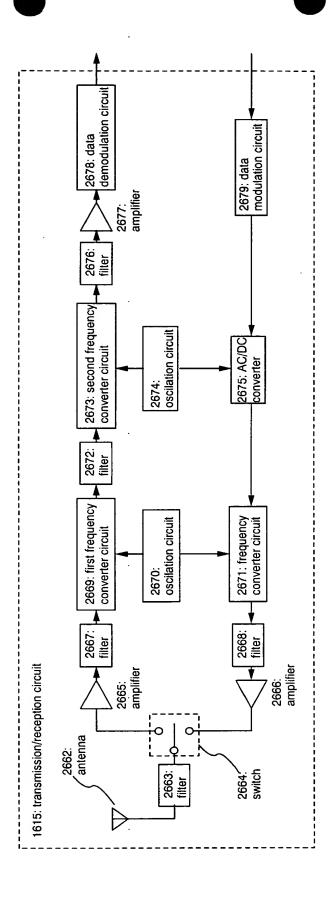


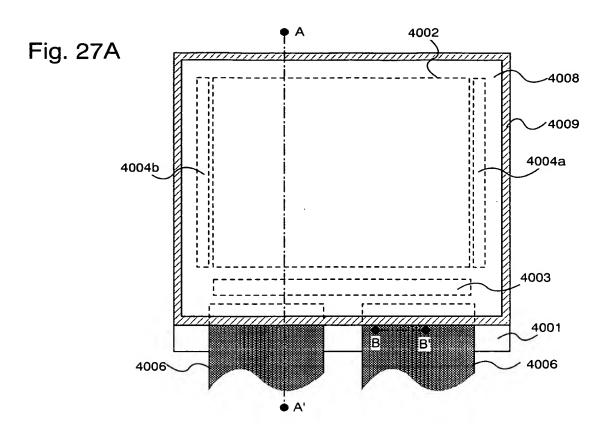


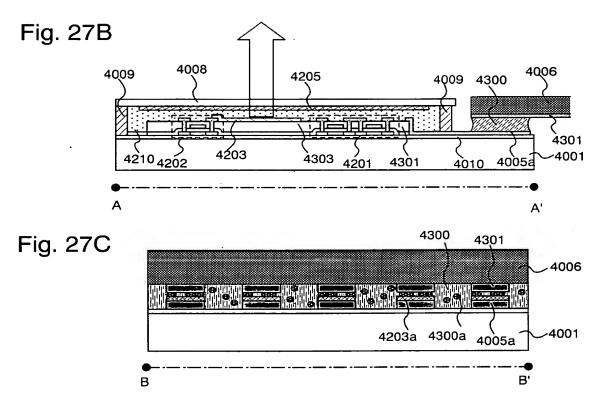


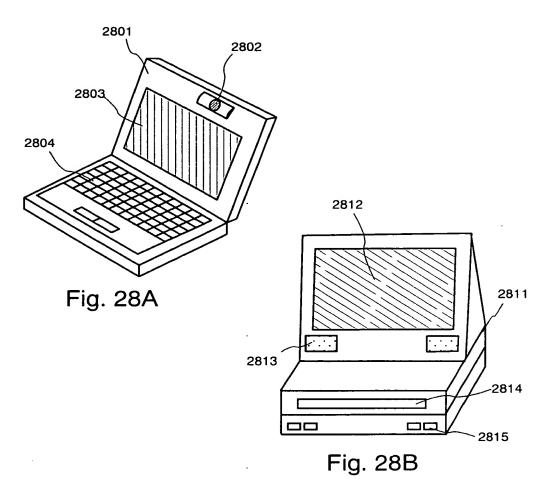


Fia. 26









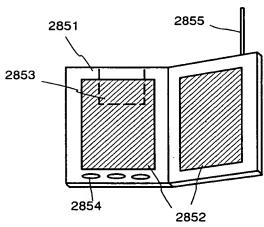


Fig. 28C

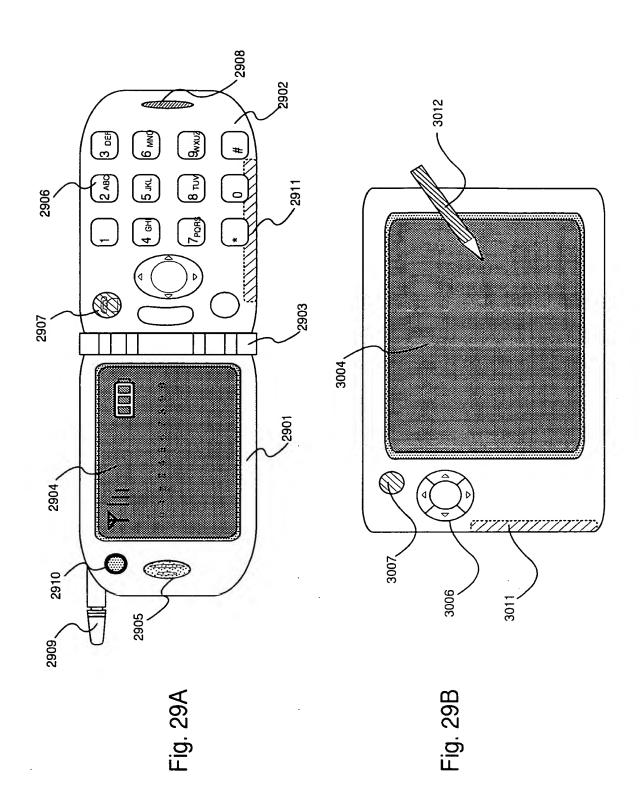


Fig. 30

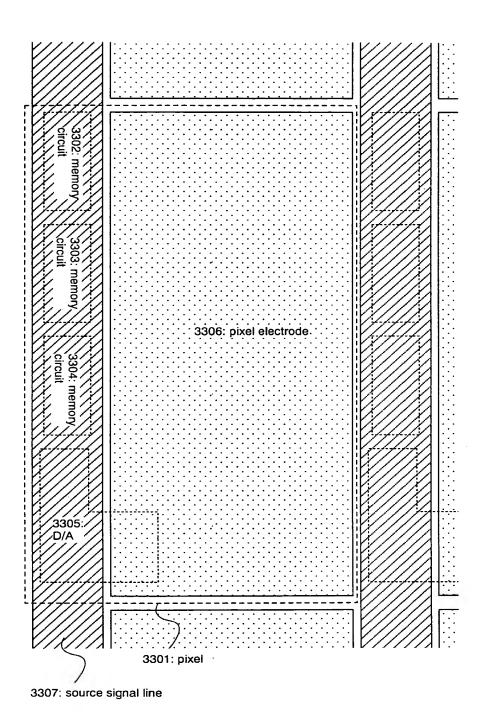


Fig. 31

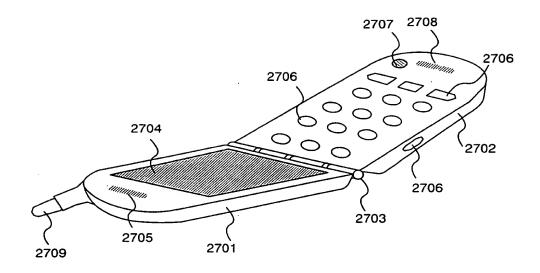


Fig. 32

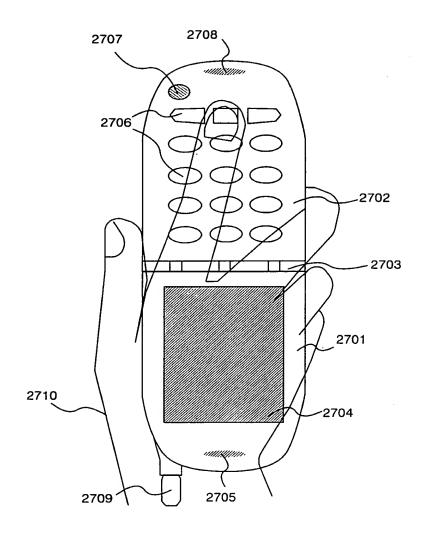
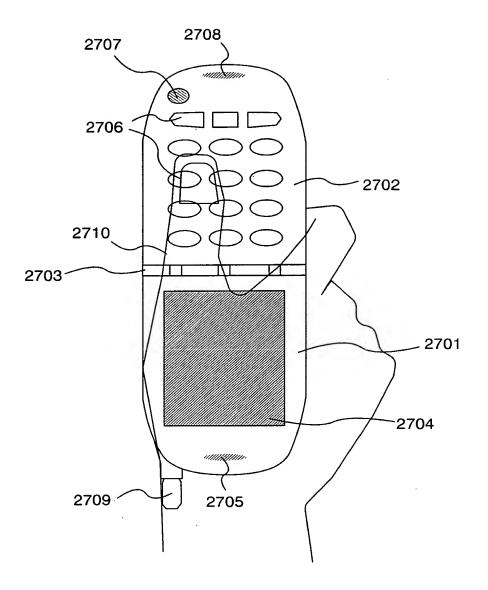


Fig. 33



source signal line driving circuit pixel portion 1513 gate signal line driving circuit 1512: LCD controller 1510: flash memory 1502: detector circuit 1501: pen touch tablet 1518: tablet interface 1509: DRAM 1507: video signal processing circuit 1503: memory circuit 1511: VRAM 1506: CPU power supply 1505: external interface port

Fig. 34 Prior Art

Fig. 35 Prior Art

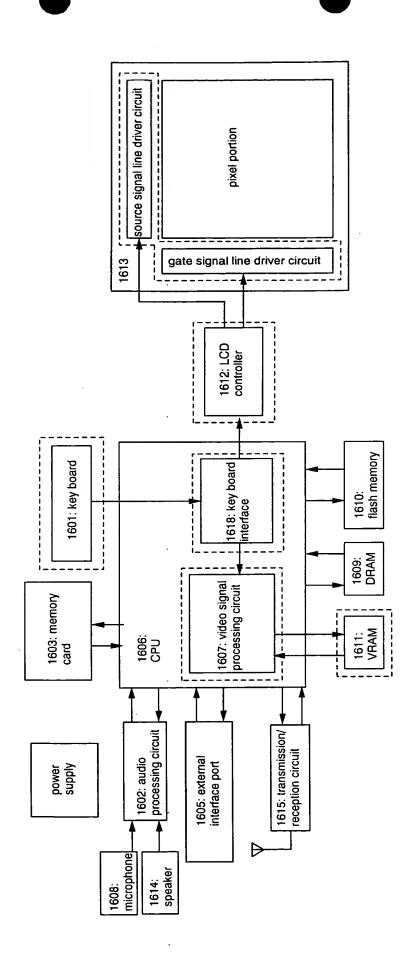


Fig. 36

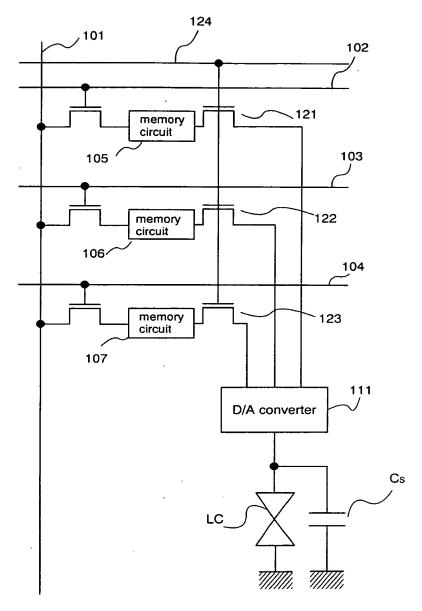


Fig. 37

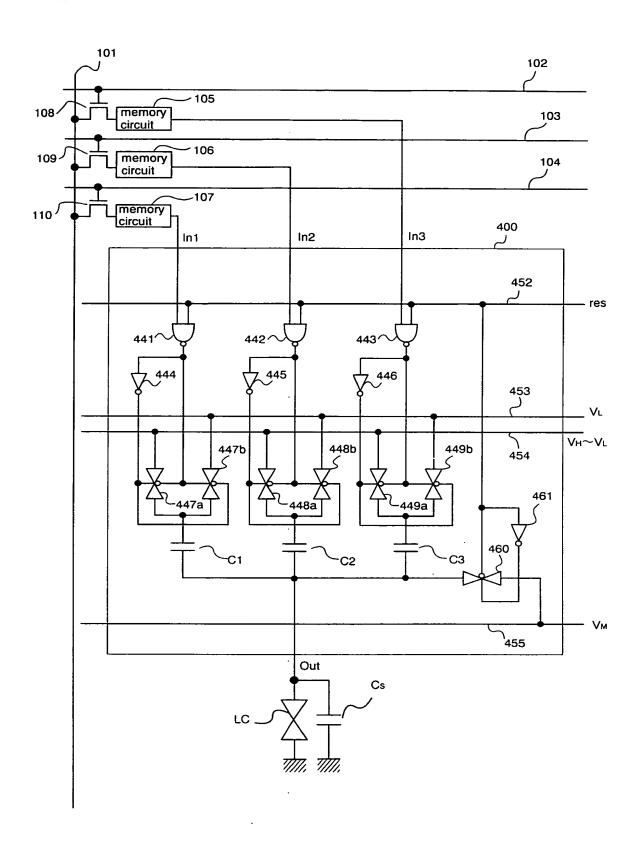


Fig. 38

